

# HA-2841

## SPICE OPERATIONAL AMPLIFIER MACRO-MODEL

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### ***Introduction***

This application note describes the SPICE macro-model for the HA-2841, a wide bandwidth op amp. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the Spice net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to help relate the SPICE listing to the schematic. The model is designed to emulate a typical rather than a worst case part. Most AC and DC parameters are simulated. Significant poles and zeros are included to give the most accurate AC and transient simulation with minimum complexity.

### ***Model Description***

#### **Input Stage**

DP and DN represent the differential input resistance. Input bias currents are created by I1 and offset current is modeled with FA. Source VN represents the input offset voltage. C1 limits slew rate. No input parasitics due to package capacitance and lead inductance are included.

#### **Gain Stage**

G2, R2, CC, GOL, and RD simulate open loop gain. CC is the macro-model dominant pole capacitor.

#### **Poles and Zeros**

The HA-2841 macro-model uses complex poles and complex zeros modeled with RLC networks plus three additional poles using RC networks.

#### **Output Stage**

EX1, D1 and D2 model output current limiting. IH and IL are the power supply currents. DPH, DPL and GPS vary the supply currents based on the opamps output current. DL, DH, ECC and EEE provide voltage clamping on the output to simulate the typical output voltage swing. Some effects of output parasitics due to package capacitance and inductance are lumped with the poles.

#### ***Parameters Not Modeled***

To maintain a simple macro-model not all op amp parameters are modeled. Most of the parameters not modeled are listed below:

- Temperature Effects
- Differential Voltage Restrictions
- Input Voltage and Current Noise
- Common Mode Restrictions
- Tolerances for Monte Carlo Analysis
- Power Supply Range

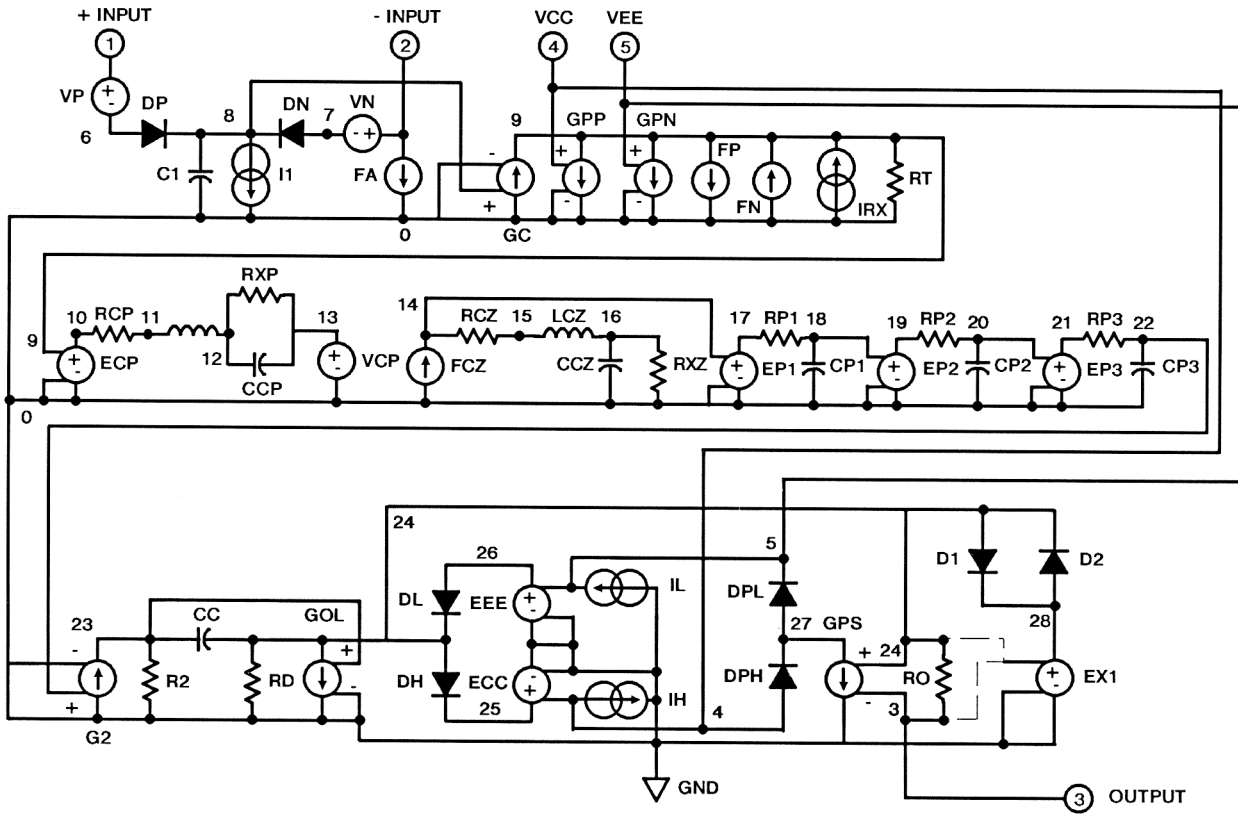
**Spice Listing**

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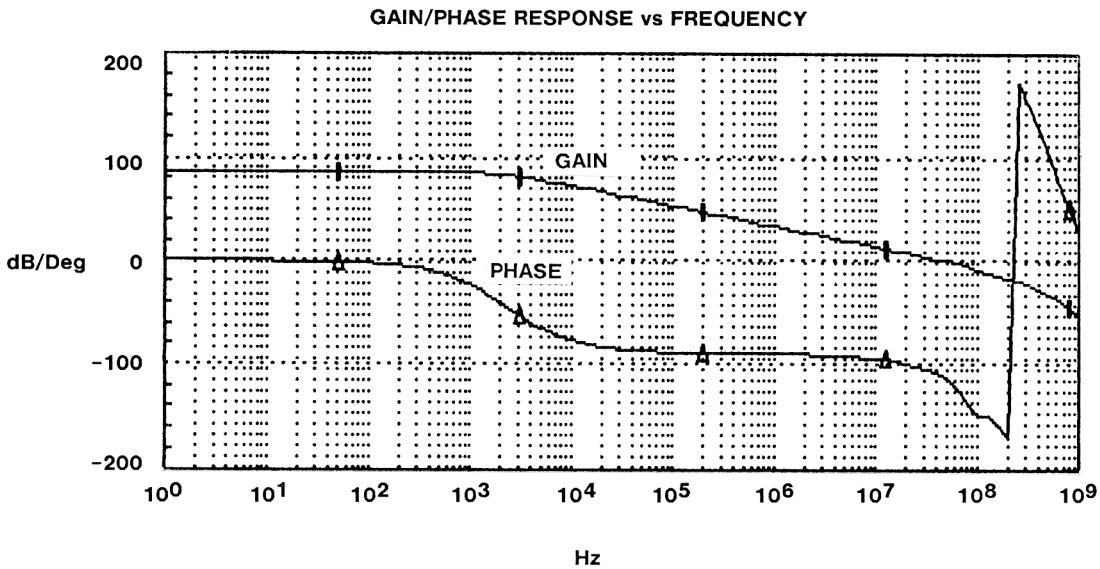
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*
*HA-2841 MACRO-MODEL
*REV: 4/22/91
*BY: D.W RIEMER
*
*PINOUT +IN -IN VCC VEE OUT
*
.SUBCKT HA2841 1 2 4 5 3
.MODEL DP D IS=1E-14 N=+1.7623E+01
.MODEL DN D IS=+7.7329E-15 N=+1.7623E+01
.MODEL DV D IS=+1.0269E-15 N=.2
.MODEL D1 D IS=1E-9 N=1
.MODEL D2 D IS=1E-9 N=+9.8971E-01
.MODEL DX D IS=1E-20 N=+30.0
*
*INPUT STAGE
*VALUE OF SOURCE VN MODELS VIO AND
MAY BE ADJUSTED AS DESIRED
*
VP 1 6 0
VN 2 7 +1.30E-03
I1 8 0 +7.9798E-06
FA 2 0 VN +5.8055E-01
DP 6 8 DP
DN 7 8 DN
C1 8 0 +3.1293E-15 IC=-9.02199
FP 9 0 VP +7.0303E+02
FN 0 9 VN +9.0914E+02
GC 0 9 8 0 +4.4083E-07
GPP 9 0 4 0 +4.4814E-07
GPN 9 0 5 0 +4.3562E-07
IRX 0 9 +4.16498E-06
RT 9 0 1.0
*
*POLES AND ZEROS
*
ECP 10 0 9 0 1.0
RCP 10 11 +8.8417E+02
LCP 11 12 +3.1272E-06
CCP 12 13 1E-12
RXP 12 13 1E+07
VCP 13 0 0.0
FCZ 0 14 VCP 1.0
RCZ 14 15 +7.7951E+02
LCZ 15 16 +2.6374E-06
CCZ 16 0 1E-12
RXZ 16 0 1E+07
EP1 17 0 14 0 1.0
RP1 17 18 +3.184
CP1 18 0 1E-10
EP2 19 0 18 0 1.0
RP2 19 20 +3.0615
CP2 20 0 1E-10
EP3 21 0 20 0 1.0
RP3 21 22 +2.6533
CP3 22 0 1E-10
*
*OUTPUT STAGE
*
G2 0 23 22 0 1.0
R2 23 0 +6.5577E+02
CC 23 24 +2.2000E-11
GOL 24 0 23 0 +2.2332E+01
RD 24 0 +2.7100E+02
DH 24 25 DV
DL 26 24 DV
ECC 25 0 POLY 1 4 0 -3.7708 1.0
EEE 26 0 POLY 1 5 0 +2.7237 1.0
IH 4 0 +9.79497E-03
IL 0 5 +9.8050E-03
GPS 27 0 24 3 +4.0000E-02
DPH 4 27 DX
DPL 27 5 DX
D1 24 28 D1
D2 28 24 D2
EX1 28 0 POLY 2 24 0 3 0 0.0 +5.9483E-01 +3.9758E-01
RO 24 3 +25.0
.ENDS HA2841

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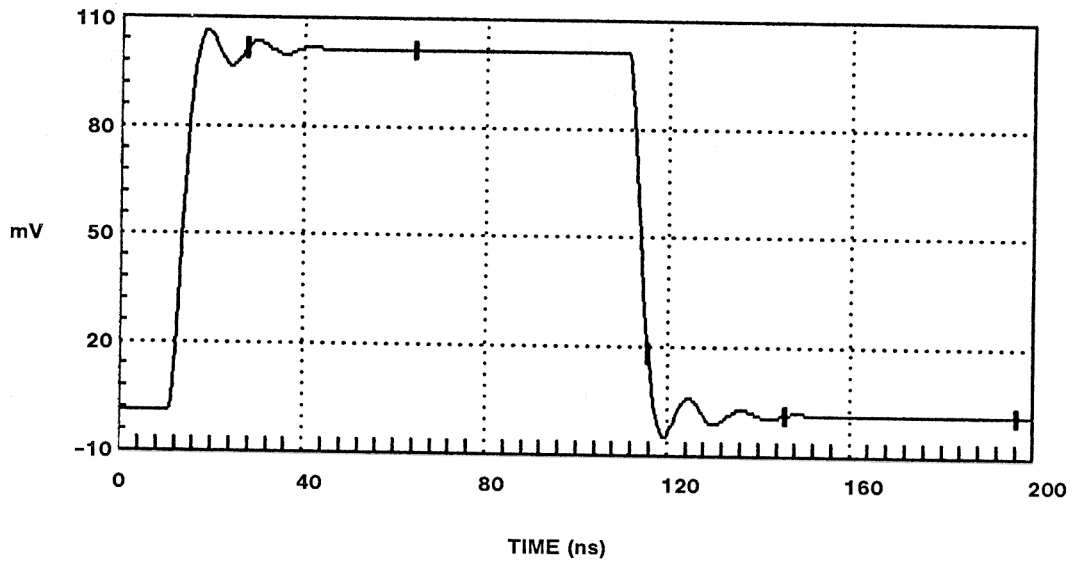
Macro-Model Schematic



Model Performance



SMALL SIGNAL RESPONSE



LARGE SIGNAL RESPONSE



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